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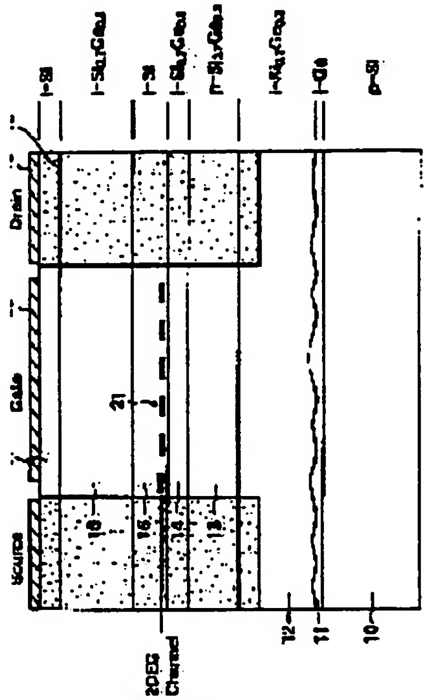

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(54) **SEMICONDUCTOR DEVICE AND ITS MANUFACTURE**

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a buffer layer having a low transition density and thin enough to plan a high speed and low power consumption device by forming the buffer layer on a second semiconductor layer and forming on the buffer layer a strain semiconductor layer having a different lattice const. from that of the buffer layer.
SOLUTION: A nondoped Ge transition conversion layer (second semiconductor layer) 11 having a surface roughness is laminated at a mean thickness of about 1 nm on a p-type Si substrate (first semiconductor layer) 10 with n-type modulation doped field effect transistors (nMOSFET) using strain Si channels, and a relaxed nondoped Si0.7Ge0.3 buffer layer (third semiconductor layer) (50 nm) 12, n-type Si0.7Ge0.3 carrier supply layer (10 nm) 13, nondoped Si0.7Ge0.3 space layer (2.5 nm) 14, nondoped strain Si channel layer (strain semiconductor layer) (10 nm) 15, nondoped Si0.7Ge0.3 cap layer (20 nm) 16 and nondoped strain Si cap layer (2 nm) 17 are laminated.

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[Claim(s)]
[Claim 1] The semiconductor device with which hauling distortion or compressive strain characterized by providing the following was applied and which is distorted and has a semiconductor layer. The 1st semiconductor layer. The 2nd semiconductor layer from which it is formed on this 1st s miconductor layer, and has irregularity on a front face, and the 1st semiconductor layer and lattice constant differ. The buffer layer formed on this 2nd semiconductor layer. The aforementioned distortion semiconductor layer from which it is formed on this buffer layer, and this buffer layer and a lattice constant differ.
[Claim 2] The semiconductor device which is characterized by providing the following, with which it pulled on the silicon substrate and distortion or compressive strain was applied and which is distorted and has an Si1-z Gez layer. The Si1-x Gex layer which is formed on the aforementioned silicon substrate and has irregularity on a front face (1>=x>0). This Si1-x Gex Si1-y Gey buffer layer formed on the layer (x!=y). This Si1-y Gey The aforementioned distortion Si1-z Gez layer formed on the layer (z!=y).
[Claim 3] The manufacture method of a semiconductor device that hauling distortion or compressive strain characterized by providing the following was applied and of it being distorted and having a semiconductor layer. The process which the 1st semiconductor layer and lattice constant differ from each other, and forms the 2nd semiconductor layer which has irregularity on a front face on the 1st semiconductor layer. The process which forms the buffer layer of an amorphous state on the 2nd semiconductor layer. The process which it anneals [process] and crystallizes the aforementioned buffer layer of an amorphous state. The process which forms the aforementioned distortion semiconductor layer from which this buffer layer and a lattice constant differ on the aforementioned buffer layer.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the semiconductor device which has the semiconductor layer to which it pulled especially on the interior or a front face, and distortion or compressive strain was applied, and its manufacture method with respect to the semiconductor device which attained improvement in the speed and low-power-ization, and its manufacture method.
[0002]
[Description of the Prior Art] Reducing power consumption is called for strongly now [when the miniaturization of electronic equipment and an information terminal advances], without an electronic device reducing a working speed. Moreover, low-power-ization of not only pocket information machines and equipment but electronic equipment is a technical problem important also from a viewpoint of environmental preservation and maintenance of an energy resource.
[0003] The conventional electronic circuitry uses Si of bulk as a substrate, and is fighting against the above-mentioned technical problem by detailed-ization of an element size. However, a physical and economical wall is visible to detailed-ization of an element, and it is necessary to establish the technology of the high speed by technique other than detailed-izing, and low-power-izing from now on.
[0004] The electronic state near the Fermi surface of undistorted Si doped by n type conventionally used for electronic devices, such as ULSI, is degenerating to six-fold. Therefore, as shown in drawing 6 , the electrons which exist in a certain valley (field of the shape of a spheroid of the constant-energy surface of the electron which is in Fermi energy EF in wave number space of field:drawing) are scattered about to other five valleys by the phonon. Such valley dispersion becomes the factor which reduces the degree of electron transfer.
[0005] On the oth r hand, it is EF, if it pulls in a field parallel to a substrate (001) to the thin film of Si and distortion is added. The electronic state which has nearby energy is divided into the ground state which degenerated doubly, and the excitation state which degenerated to four-fold. Almost all electrons remain in the ground state which carried out double degeneracy in the state where an electronic

distribution does not separate extremely from a Fermi distribution (when high electric field are not mark-ized etc.). Consequently, electronic valley dispersion is restricted to disp rsion between another valleys. Consequently, the mobility in field inboard rises. When Si layer to which was followed, for example, hauling distortion was added is used for the channel of n-MOSFET, a bird clapper is expected that high-sp ed operation is conventionally more possible than an element.

[0006] On the other hand, when the compressive-strain SiGe layer formed on this distortion Si layer and Si substrate is used as an electron hole channel, it is pointed out according to the effect which r duction of electron hole mass and degeneracy of a valence band solve that the mobility of an electron hole improves too. Consequently, improvement in working speeds, such as p-MOSFET and n-MODFET, is expectable. It is of the same grade as the conventional Si element that it is important in any case, or it is that the high-speed operation more than Si is expectable also in the operating voltage not more than it. This shows possibility that it is compatible in high-speed operation and low-power-ization.

[0007] Hauling distortion Si is obtained by growing Si epitaxially on the big crystal of a lattice constant rather than Si. Usually, the SiGe buffer layer which carried out grid relief is grown up on Si substrate, and Si thin film is grown up on it.

[0008] However, in order to obtain the SiGe front face of low dislocation density which carried out grid r lief, the thick buffer layer which amounts to several micrometers was required. It is because compressive strain remain on the front face of a SiGe layer, the amount of distortion obtained is not enough, or problems, like dislocation density is high arise even when grid relief is enough, when a buffer layer is thin. However, in formation of a thick buffer layer, the problem that a throughput decreases [dozens of minutes - several hours and very long time] for this reason occurs.

[0009] moreover, several micrometers big **** according to a thick SiGe buffer layer when it is going to form a distortion Si element field and the usual Si-MOS field on the same substrate -- being generated -- lithography and an electrode -- **** -- ** -- the problem of causing difficulty was in the process

[0010] Moreover, as the technique of reducing a parasitic capacitance and attaining improvement in the speed, although the element creation technology to a SOI substrate top is used, the adjustment with this technology of a thick SiGe buffer layer is also bad in recent years. That is, pn junction area increases after all by existence of a thick SiGe buffer layer, a parasitic capacitance increases, and the meaning using a SOI substrate is lost.

[0011] Moreover, the dislocation density in a SiGe buffer-layer front face shows the big value of 104 -107 cm-2. This value is still insufficient for producing a realistic element, especially an integration element.

[0012] In especially production of an integration element, a demand becomes severe further from the homogeneous point of the yield and a property, and it is necessary to suppress dislocation density less than [1.0x103 cm-2]. However, in a Prior art, the dislocation density in a SiGe buffer-layer front face shows the very large value of 104 -107 cm-2, and realization of an integration element is difficult.

[0013]

[Problem(s) to be Solved by the Invention] Since a throughput would become low if a thick SiGe buffer layer is formed as mentioned above, there was a problem that a manufacturing cost increased. Moreover, since a big level difference arose that it is a thick buffer layer, there was a problem that processes, such as lithography and electrode formation, were difficult.

[0014] Moreover, although the transition density of a buffer layer needed to be suppressed less than [1.0x103 cm-2], the dislocation density in the SiGe buffer-layer front face obtained with the conventional technology shows the very large value of 104 -107 cm-2, and realization of an integration element had the problem of being difficult.

[0015] It is distorted, has a semiconductor layer, and has low transition density and a sufficiently thin buffer layer, and the purpose of this invention is to offer the semiconductor device with which hauling distortion or compressive strain was applied and which can attain improvement in the speed and low-power-ization, and its manufacture method.

[0016]

[Means for Solving the Problem] [Composition] this invention is constituted as follows, in order to attain the above-mentioned purpose.

(1) The semiconductor device of this invention (claim 1) It is the semiconductor device with which

hauling distortion or compressive strain was applied and which is distorted and has a semiconductor layer. The 1st semiconductor layer, The 2nd semiconductor layer from which it is formed on this 1st s miconductor layer, and has irregularity on a front face, and the 1st semiconductor layer and lattice constant differ, The buffer layer formed on this 2nd semiconductor layer and the aforementioned distortion s miconductor layer from which it is formed on this buffer layer, and this buffer layer and a lattice constant differ are provided, and it is characterized by the bird clapper.
[0017] A distortion semiconductor layer is used as an electron or a run channel of an electron hole.
(2) The semiconductor device of this invention (claim 2) Distortion Si1-z Gez to which it pulled on the silicon substrate and distortion or compressive strain was applied The Si1-x Gex layer which is the semiconductor device which has a layer, is formed on the aforementioned silicon substrate, and has irregularity on a front face (1>=x>0), This Si1-x Gex The Si1-y Gey buffer layer (x!=y) formed on the layer, and this Si1-y Gey The aforementioned distortion Si1-z Gez layer (z!=y) formed on the layer is provided, and it is characterized by the bird clapper.
[0018] It is desirable that they are x>y>z or x>y, and z>y. As for the average thickness of an Si1-x Gex layer (1>=x>0), it is desirable that it is 1-5nm.
[0019] Si1-z Gez A layer is used as an electron or a run channel of an electron hole.
(3) The manufacture method of the semiconductor device of this invention (claim 3) The process which it is the manufacture method of a semiconductor device that hauling distortion or compressive strain was applied and of it being distorted and having a semiconductor layer, and the 1st semiconductor layer and lattice constant differ from each other on the 1st semiconductor layer, and forms in a front face the 2nd semiconductor layer which has irregularity, It is characterized by including the process which forms the buffer layer of an amorphous state on the 2nd semiconductor layer, the process which it anneals [process] and crystallizes the aforementioned buffer layer of an amorphous state, and the process which forms the aforementioned distortion semiconductor layer from which this buffer layer and a lattice constant differ on the aforementioned buffer layer.
[0020] The 2nd semiconductor layer which has irregularity is formed in a front face of island-like growth. The 1st semiconductor layer is a silicon substrate and the 2-4th semiconductor layers are an Si1-x Gex layer (1>=x>0), an Si1-y Gey layer (x!=y), and an Si1-z Gez layer (z!=y), respectively.
[0021] A silicon substrate and the Si1-x Gex layer which is formed on this silicon substrate and has irregularity on a front face (1>=x>0), Si1-x Gex The Si1-y Gey (x!=y) layer formed on the layer, Si1-z1Gez1 (z1!=y) layer formed on the predetermined field of this Si1-y Gey layer (x!=y), It comes to provide Si1-z2Gez2 formed in the field in which Si1-z1Gez1 (z1!=y) layer on the aforementioned Si1-y Gey layer (x!=y) is not formed. In addition, aforementioned Si1-z1Gez1 and Si1-z2Gez2 work as a conduction channel of reversed polarity.
[0022] A [operation] this invention has the following operation and effects by the above-mentioned composition. If the 2nd semiconductor layer which has irregularity on a front face is formed on the 1st semiconductor layer, distortion will be accumulated in the border area of heights and heights, and it will become the situation that a crystal defect tends to enter. If the buffer layer of an amorphous state is besides deposited and annealed, crystallization will begin from the field which is in contact with the 2nd semiconductor layer. The strain energy accumulates the buffer layer as crystallization progresses, since the lattice constant is larger than the 2nd semiconductor layer. If a critical value with strain energy is exceeded, transition will arise from the interface of a crystal layer and an amorphous layer towards the 2nd semiconductor layer [near / aforementioned / the border area].
[0023] Furthermore, if crystallization progresses, as the border area of heights and heights is sewn taking advantage of this transition, transition will arise in a substrate in parallel. Consequently, an island-like structure field can be made to generate transition with high density in parallel in a substrate, after stopping low the density of penetration transition which arrives at the front face of a crystal layer. Since the difference of the lattice constant of a buffer layer and the 1st semiconductor layer is absorbed by transition, the buffer layer enough eased by low dislocation density is obtained.
[0024] Moreover, when it grows epitaxially directly and a buffer layer is formed on the 2nd semiconductor layer which has irregularity, irregularity will be formed on the surface of a buffer layer, and the process which carries out flattening of the front face is needed. However, after forming the buffer layer in the amorphous state where the irregularity of a ground is not reflected, like this invention, a buffer layer with a flat front face is easily obtained by crystallizing a buffer layer.

[0025]
[Embodiments of the Invention] The gestalt of operation of this invention is explained with reference to a drawing below.
[1st operation gestalt] drawing 1 is the cross section showing the important section composition of the semiconductor device concerning the 1st operation gestalt of this invention. This operation gestalt is n type modulation dope field-effect transistor (nMODFET) which used the distorted Si channel.
[0026] germanium transition conversion layer (the 2nd semiconductor layer, Si1-x Gex layer (1>=x>0)) 11 of the non dope which has irregularity on a front face on the p type Si substrate (1st semiconductor layer) 10 6ML(s) (about 1nm in average thickness), Eased non dope Si0.7 germanium0.3 Buffer layer () [the 3rd semiconductor layer,] [Si1-y] The Gey layer (x!=y) (50nm) 12 and n type Si0.7 germanium0.3 spacer layer (2.5nm) 14, non dope distorted Si channel layer The carrier supply layer (n= 4.0x1018cm -3 or 10nm) 13 and non dope Si0.7 germanium0.3 (a distortion semiconductor layer and Si1-z Gez ()) The z!=y layer (10nm) 15 and non dope Si0.7 germanium0.3 The laminating of the cap layer (20nm) 16 and the non dope distorted Si cap layer 17 (2nm) is carried out one by one.
[0027] Si cap layer 17 - Si0.7 germanium0.3 The source and the drain which consist of an aluminum electrode 19 formed on ion implantation, n type diffusion field 18 formed of annealing, and n type diffusion field 18 are formed in the laminated structure of a buffer layer 12. The Schottky gate electrode 20 constituted by Pt (20nm) / Ti (20nm) / aluminum (200nm) is formed in the field inserted into the aluminum electrode 19 on Si cap layer 17.
[0028] In this operation gestalt, the distortion by the grid mismatching between the Si substrate 10 and a buffer layer 12 is absorbed by the transition conversion layer 11 by transition produced in parallel at a substrate 10, and is eased completely substantially. Therefore, sufficient hauling distortion for the distorted Si channel 15 is added, and the two-dimensional electron gas channel 21 is formed near the interface of the spacer layer 14 and a channel 15.
[0029] Next, the manufacture method of the semiconductor device of drawing 1 is explained using the process cross section of drawing 2 . First, as shown in drawing 2 (a), on the Si substrate 10, 6ML supply of the germanium is carried out by CVD, and germanium transition conversion layer 11 with an average thickness of 1nm is formed. In addition, substrate temperature is 500 degrees C. Since germanium transition conversion layer 11 grows in the shape of an island by grid mismatching with a substrate, the structure which about [base 20nmx20-100nm height 2nm] island-like structure adjoined mutually, and was close is formed. Therefore, irregularity is formed in the front face of germanium transition conversion layer 11 as shown in the thickness distribution of drawing 3 . In addition, the thickness distribution of drawing 3 is the result of being obtained by AFM.
[0030] The state of the island-like structure of germanium transition conversion layer 11 is shown in drawing 4 . As shown in drawing 4 , although near the summit of the island of germanium transition conversion layer 11 can ease distortion to some extent by deformation of a longitudinal direction, stress concentrates it on the border area 30 with a pars basilaris ossis occipitalis, especially the next island.
[0031] Subsequently, the partial pressure of the disilane which is material gas is increased to 1Pa, and it is amorphous non dope Si0.7 germanium0.3. 50nm grows a layer 31. And the temperature up of the substrate temperature is carried out to 600 degrees C, and it anneals for 10 minutes in hydrogen atmosphere. If annealing is started, as shown in drawing 2 (b), crystallization is started from the amorphous layer 31 of the portion which is in contact with the germanium layer 11, and the crystal layer 32 is formed. If the crystal layer 32 is set to about several nm, the penetration transition 33 will arise into the weak portion of the border areas 10 especially. Furthermore, if the crystal layer 32 grows, as are shown in drawing 2 (c), and the border area of germanium island is sewn, the penetration transition 33 will be formed in the direction parallel to a substrate in the shape of a mesh.
[0032] Subsequently, non dope Si0.7 germanium0.3 which the amorphous layer crystallized complet ly and was eased If a buffer layer 12 is formed, as shown in drawing 2 (d), a disilane partial pressure will b returned to the usual epitaxial growth conditions (2.5xl0-2Pa), and the laminating of the carrier supply layer 13, the spacer layer 14, the channel layer 15, and the cap layers 16 and 17 will be carried out one by one.
[0033] Then, although the source, a drain, and the gate are formed in a wafer by ion implantation or metallization and FET is mad , since these manufacture processes are generally used well, detail d explanation is omitted. However, it is necessary to suppress the upper limit temperatur of a process at

about 850 degrees C so that a distortion silicon layer may ease and transition may not occur.
[0034] In addition, in this operation gestalt, although the top used the usual CVD growth from the carrier supply layer, it is also possible for it to be amorphous, to form all the layers by the side of a front face from the start, and to crystallize from the transition conversion layer 11.
[0035] [2nd operation g stalt] drawing 5 is the cross section showing the important section composition of the semiconductor device concerning the 2nd operation gestalt of this invention. In addition, in drawing 5 , the same sign is given to the same portion as drawing 1 , and the detailed explanation is omitted. The semiconductor device of this operation gestalt is the CMOS inverter which used the distorted Si layer as p and an n channel.
[0036] n type germanium transition conversion layer 11a, n type relief Si0.7 germanium0.3-layer 12a, and n type distortion silicon layer 15a are formed on the n type Si substrate 10. And p type well is formed in a predetermined field of ion implantation, and it is p type germanium transition conversion layer 11b and p type relief Si0.7 germanium0.3. Layer 12b and p type distortion silicon layer 15b are formed. In addition, 55 is an insulator layer.
[0037] moreover, CMOS **** shown in drawing 5 -- bias of source 51a of pMOS and the n type relief layer 12a is carried out to 3V through wiring 57a, and source 52a of nMOS and p type relief layer 12b are connected to the ground through wiring 57c An input is applied to the gates 54a and 54b of both MOSs, and drain 51b of pMOS and drain 51b of nMOS become an output.
[0038] Since CMOS is the same composition as what is used for usual Si-CMOS except the structure of a substrate, it omits detailed explanation.
The [3rd operation gestalt] book operation gestalt shows the example using the MOS structure (HMOS) which has a channel at a hetero interface to a change of the usual MOS structure.
[0039] Drawing 6 is the cross section showing the important section composition of the semiconductor device which has the HMOS structure concerning the 3rd operation gestalt of this invention. In addition, in drawing 6 , the same sign is given to drawing 1 and the same portion as 5, and the detailed explanation is omitted.
[0040] What is necessary is just to insert p type distorted Si0.3 germanium0.7 layer (compressive strain) 61b of 5nm thickness between distorted Si layer 15b and the gate oxide film 53 about n-HMOS. p-HMOS -- being related -- n type Si0.3 germanium0.7 of 10nm of thickness of nHMOS and common use Layer 61a and distorted Si layer (hauling distortion) of 5nm of thickness 62a are inserted. [between / distorted Si layer 15a and the gate oxide films 53] In addition, it is distorted with distortion layer 61a, and the difference in thickness with layer 61b is a part to have been consumed by formation of the gate oxide film 53 of n-HMOS.
[0041] In this case, an n channel is distorted Si layer 15b and distorted Si0.3 germanium0.7. Near an interface with layer 61b, a p channel is distorted Si0.3 germanium0.7 again. It is formed between layer 61a and distorted Si layer 62a, respectively.
[0042] As a modification of this operation gestalt, it can also be fastidious using modulation dope structure as shown in the 1st operation gestalt. In this case, it is Si0.3 germanium0.7 to the upper part of p and an n channel. A spacer layer is minded and they are p type and n type Si0.3 germanium0.7. It is necessary to add a carrier supply layer.
[0043] In addition, this invention is not limited to the above-mentioned operation gestalt. For example, as a transition conversion layer, what is necessary is just Si1-x Gex (1>=x>0). Moreover, as a buffer layer, what is necessary is just Si1-y Gey (x!=y). Moreover, as a channel layer, what is necessary is just Si1-z Gez (z!=y).
[0044] Besides the combination mentioned above, GaAs(1st semiconductor layer)/InAs(2nd semiconductor layer)/InGaAs(3rd semiconductor layer)/InGaAs (distortion semiconductor layer), GaAs(1st semiconductor layer)/InP(2nd semiconductor layer)/InGaAsP(3rd semiconductor layer)/InGaAs (distortion semiconductor layer), Combination, such as InP(1st semiconductor layer)/InGaP(2nd semiconductor layer)/InGaP(3rd semiconductor layer)/InGaAs (distortion semiconductor lay r), is possible. In addition, this invention is th range which does not d viat from th summary, and it deforms variously and it can be carried out.
[0045]
[Effect of the Invention] As explained above, according to this invention, it excels in productivity and small distortion Si of transition density or a SiGe layer is obtained rather than before. Consequently, a

low power and high-speed operation become possible from the conventional Si electronic device.

[Translation don .]
TECHNICAL FIELD

[The technical field to which invention belongs] this invention relates to the semiconductor device which has the semiconductor layer to which it pulled especially on the interior or a front face, and distortion or compressive strain was applied, and its manufacture method with respect to the semiconductor device which attained improvement in the speed and low-power-ization, and its manufacture method.

[Translation done.]
PRIOR ART

[Description of the Prior Art] Reducing power consumption is called for strongly now [when the miniaturization of electronic equipment and an information terminal advances], without an electronic device reducing a working speed. Moreover, low-power-ization of not only pocket information machines and equipment but electronic equipment is a technical problem important also from a viewpoint of environmental preservation and maintenance of an energy resource.
[0003] The conventional electronic circuitry uses Si of bulk as a substrate, and is fighting against the above-mentioned technical problem by detailed-ization of an element size. However, a physical and economical wall is visible to detailed-ization of an element, and it is necessary to establish the technology of the high speed by technique other than detailed-izing, and low-power-izing from now on.
[0004] The electronic state near the Fermi surface of undistorted Si doped by n type conventionally used for electronic devices, such as ULSI, is degenerating to six-fold. Therefore, as shown in drawing 6, the electrons which exist in a certain valley (field of the shape of a spheroid of the constant-energy surface of the electron which is in Fermi energy EF in wave number space of field:drawing) are scattered about to other five valleys by the phonon. Such valley dispersion becomes the factor which reduces the degree of electron transfer.
[0005] On the other hand, it is EF, if it pulls in a field parallel to a substrate (001) to the thin film of Si and distortion is added. The electronic state which has nearby energy is divided into the ground state which degenerated doubly, and the excitation state which degenerated to four-fold. Almost all electrons remain in the ground state which carried out double degeneracy in the state where an electronic distribution does not separate extremely from a Fermi distribution (when high electric field are not mark-ized etc.). Consequently, electronic valley dispersion is restricted to dispersion between another valleys. Consequently, the mobility in field inboard rises. When Si layer to which was followed, for example, hauling distortion was added is used for the channel of n-MOSFET, a bird clapper is expected that high-speed operation is conventionally more possible than an element.
[0006] On the other hand, when the compressive-strain SiGe layer formed on this distortion Si layer and Si substrate is used as an electron hole channel, it is pointed out according to the effect which reduction of electron hole mass and degeneracy of a valence band solve that the mobility of an electron hole improves too. Consequently, improvement in working speeds, such as p-MOSFET and n-MODFET, is expectable. It is of the same grade as the conventional Si element that it is important in any case, or it is that the high-speed operation more than Si is expectable also in the operating voltage not more than it. This shows possibility that it is compatible in high-speed operation and low-power-ization.
[0007] Hauling distortion Si is obtained by growing Si epitaxially on the big crystal of a lattice constant rather than Si. Usually, the SiGe buffer layer which carried out grid relief is grown up on Si substrate, and Si thin film is grown up on it.
[0008] However, in ord r to obtain the SiGe front face of low dislocation density which carried out grid relief, the thick buffer layer which amounts to several micrometers was required. It is because

compressive strain remain on the front face of a SiGe layer, the amount of distortion obtained is not enough, or problems, like dislocation density is high arise even when grid relief is enough, when a buffer layer is thin. However, in formation of a thick buffer layer, the problem that a throughput decreases [dozens of minut s - several hours and very long time] for this reason occurs.
[0009] moreov r, s veral micrometers big **** according to a thick SiGe buffer layer when it is going to form a distortion Si element field and the usual Si-MOS field on the same substrate -- being generated -- lithography and an electrode -- **** -- ** -- the problem of causing difficulty was in the process
[0010] Moreover, as the technique of reducing a parasitic capacitance and attaining improvement in the speed, although the element creation technology to a SOI substrate top is used, the adjustment with this technology of a thick SiGe buffer layer is also bad in recent years. That is, pn junction area increases after all by existence of a thick SiGe buffer layer, a parasitic capacitance increases, and the meaning using a SOI substrate is lost.
[0011] Moreover, the dislocation density in a SiGe buffer-layer front face shows the big value of 104 - 107 cm-2. This value is still insufficient for producing a realistic element, especially an integration element.
[0012] In especially production of an integration element, a demand becomes severe further from the homogeneous point of the yield and a property, and it is necessary to suppress dislocation density less than [1.0x103 cm-2]. However, in a Prior art, the dislocation density in a SiGe buffer-layer front face shows the very large value of 104 -107 cm-2, and realization of an integration element is difficult.

[Translation done.]
EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, according to this invention, it excels in productivity and small distortion Si of transition density or a SiGe layer is obtained rather than before. Consequently, a low power and high-speed operation become possible from the conventional Si electronic device.

[Translation done.]
TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Since a throughput would become low if a thick SiGe buffer layer is formed as mentioned above, there was a problem that a manufacturing cost increased. Moreover, since a big level difference arose that it is a thick buffer layer, there was a problem that processes, such as lithography and electrode formation, were difficult.
[0014] Moreover, although the transition density of a buffer layer needed to be suppressed less than [1.0x103 cm-2], the dislocation density in the SiGe buffer-layer front face obtained with the conventional technology shows the very large value of 104 -107 cm-2, and realization of an integration element had the problem of being difficult.
[0015] It is distorted, has a semiconductor layer, and has low transition density and a sufficiently thin buffer layer, and the purpose of this invention is to offer the semiconductor device with which hauling distortion or compressive strain was applied and which can attain improvement in the speed and low-power-ization, and its manufacture method.

[Translation done.]
MEANS

[Means for Solving the Problem] [Composition] this invention is constituted as follows, in order to attain the above-mentioned purpose.

(1) As for the semiconductor device of this invention (claim 1), this invention is characterized by the semiconductor device with which hauling distortion or compressive strain was applied and which is distorted and has a semiconductor layer possessing the following. The 1st semiconductor layer. The 2nd semiconductor layer from which it is formed on this 1st semiconductor layer, and has irregularity on a front face, and the 1st semiconductor layer and lattice constant differ. The buffer layer formed on this 2nd semiconductor layer. The aforementioned distortion semiconductor layer from which it is formed on this buffer layer, and this buffer layer and a lattice constant differ.
[0017] A distortion semiconductor layer is used as an electron or a run channel of an electron hole.
(2) For this invention, the semiconductor device of this invention (claim 2) is distortion Si1-z Gez to which it pulled on the silicon substrate and distortion or compressive strain was applied. The semiconductor device which has a layer is characterized by providing the following. The Si1-x Gex layer which is formed on the aforementioned silicon substrate and has irregularity on a front face (1>=x>0). This Si1-x Gex Si1-y Gey buffer layer formed on the layer (x!=y). This Si1-y Gey The aforementioned distortion Si1-z Gez layer formed on the layer (z!=y).
[0018] It is desirable that they are x>y>z or x>y, and z>y. As for the average thickness of an Si1-x Gex layer (1>=x>0), it is desirable that it is 1-5nm.
[0019] Si1-z Gez A layer is used as an electron or a run channel of an electron hole.
(3) As for the manufacture method of the semiconductor device of this invention (claim 3), this invention is characterized by the manufacture method of a semiconductor device that hauling distortion or compressive strain was applied and of it being distorted and having a semiconductor layer possessing the following. The process which the 1st semiconductor layer and lattice constant differ from each other, and forms the 2nd semiconductor layer which has irregularity on a front face on the 1st semiconductor layer. The process which forms the buffer layer of an amorphous state on the 2nd semiconductor layer. The process which it anneals [process] and crystallizes the aforementioned buffer layer of an amorphous state. The process which forms the aforementioned distortion semiconductor layer from which this buffer layer and a lattice constant differ on the aforementioned buffer layer.
[0020] The 2nd semiconductor layer which has irregularity is formed in a front face of island-like growth. The 1st semiconductor layer is a silicon substrate and the 2-4th semiconductor layers are an Si1-x Gex layer (1>=x>0), an Si1-y Gey layer (x!=y), and an Si1-z Gez layer (z!=y), respectively.
[0021] A silicon substrate and the Si1-x Gex layer which is formed on this silicon substrate and has irregularity on a front face (1>=x>0), Si1-x Gex The Si1-y Gey (x!=y) layer formed on the layer, Si1-z1Gez1 (z1!=y) layer formed on the predetermined field of this Si1-y Gey layer (x!=y), It comes to provide Si1-z2Gez2 formed in the field in which Si1-z1Gez1 (z1!=y) layer on the aforementioned Si1-y Gey layer (x!=y) is not formed. In addition, aforementioned Si1-z1Gez1 and Si1-z2Gez2 work as a conduction channel of reversed polarity.

[Translation done.]

OPERATION

A [operation] this invention has the following operation and effects by the above-mentioned composition. If the 2nd semiconductor layer which has irregularity on a front face is formed on the 1st semiconductor layer, distortion will be accumulated in the border area of heights and heights, and it will become the situation that a crystal defect tends to enter. If the buffer layer of an amorphous state is besides deposited and annealed, crystallization will begin from the field which is in contact with the 2nd semiconductor layer. The strain energy accumulates the buffer layer as crystallization progresses, since the lattice constant is larger than the 2nd semiconductor layer. If a critical value with strain energy is exceeded, transition will arise from the interface of a crystal layer and an amorphous layer towards the 2nd semiconductor layer [near / aforementioned / the border area].
[0023] Furthermore, if crystallization progresses, as the border area of heights and heights is sewn taking advantage of this transition, transition will arise in a substrate in parallel. Consequently, an

island-lik structure field can be made to generate transition with high density in parallel in a substrate, after stopping low the density of penetration transition which arrives at the front face of a crystal layer. Since the difference of the lattic constant of a buffer layer and the 1st semiconductor layer is absorbed by transition, the buffer layer enough eased by low dislocation density is obtained.
[0024] Moreover, when it grows epitaxially directly and a buffer layer is formed on the 2nd semiconductor layer which has irregularity, irregularity will be formed on the surface of a buffer layer, and the process which carries out flattening of the front face is needed. However, after forming the buffer layer in the amorphous state where the irregularity of a ground is not reflected, like this invention, a buffer layer with a flat front face is easily obtained by crystallizing a buffer layer.
[0025]
[Embodiments of the Invention] The gestalt of operation of this invention is explained with reference to a drawing below.
[1st operation gestalt] drawing 1 is the cross section showing the important section composition of the semiconductor device concerning the 1st operation gestalt of this invention. This operation gestalt is n type modulation dope field-effect transistor (nMODFET) which used the distorted Si channel.
[0026] germanium transition conversion layer (the 2nd semiconductor layer, Si1-x Gex layer (1>=x>0)) 11 of the non dope which has irregularity on a front face on the p type Si substrate (1st semiconductor layer) 10 6ML(s) (about 1nm in average thickness), Eased non dope Si0.7 germanium0.3 Buffer layer () [the 3rd semiconductor layer,] [Si1-y] The Gey layer (x!=y) (50nm) 12 and n type Si0.7 germanium0.3 spacer layer (2.5nm) 14, non dope distorted Si channel layer The carrier supply layer (n= 4.0x1018cm -3 or 10nm) 13 and non dope Si0.7 germanium0.3 (a distortion semiconductor layer and Si1-z Gez ()) The z!=y layer (10nm) 15 and non dope Si0.7 germanium0.3 The laminating of the cap layer (20nm) 16 and the non dope distorted Si cap layer 17 (2nm) is carried out one by one.
[0027] Si cap layer 17 - Si0.7 germanium0.3 The source and the drain which consist of an aluminum electrode 19 formed on ion implantation, n type diffusion field 18 formed of annealing, and n type diffusion field 18 are formed in the laminated structure of a buffer layer 12. The Schottky gate electrode 20 constituted by Pt (20nm) / Ti (20nm) / aluminum (200nm) is formed in the field inserted into the aluminum electrode 19 on Si cap layer 17.
[0028] In this operation gestalt, the distortion by the grid mismatching between the Si substrate 10 and a buffer layer 12 is absorbed by the transition conversion layer 11 by transition produced in parallel at a substrate 10, and is eased completely substantially. Therefore, sufficient hauling distortion for the distorted Si channel 15 is added, and the two-dimensional electron gas channel 21 is formed near the interface of the spacer layer 14 and a channel 15.
[0029] Next, the manufacture method of the semiconductor device of drawing 1 is explained using the process cross section of drawing 2 . First, as shown in drawing 2 (a), on the Si substrate 10, 6ML supply of the germanium is carried out by CVD, and germanium transition conversion layer 11 with an average thickness of 1nm is formed. In addition, substrate temperature is 500 degrees C. Since germanium transition conversion layer 11 grows in the shape of an island by grid mismatching with a substrate, the structure which about [base 20nmx20-100nm height 2nm] island-like structure adjoined mutually, and was close is formed. Therefore, irregularity is formed in the front face of germanium transition conversion layer 11 as shown in the thickness distribution of drawing 3 . In addition, the thickness distribution of drawing 3 is the result of being obtained by AFM.
[0030] The state of the island-like structure of germanium transition conversion layer 11 is shown in drawing 4 . As shown in drawing 4 , although near the summit of the island of germanium transition conversion layer 11 can ease distortion to some extent by deformation of a longitudinal direction, stress concentrates it on the border area 30 with a pars basilaris ossis occipitalis, especially the next island.
[0031] Subsequently, the partial pressure of the disilane which is material gas is increased to 1Pa, and it is amorphous non dope Si0.7 germanium0.3. 50nm grows a layer 31. And the temperature up of the substrate temperatur is carried out to 600 degrees C, and it anneals for 10 minutes in hydrogen atmosphere. If annealing is started, as shown in drawing 2 (b), crystallization is started from the amorphous layer 31 of th portion which is in contact with the germanium layer 11, and the crystal layer 32 is formed. If the crystal layer 32 is set to about several nm, the penetration transition 33 will arise into the weak portion of the border areas 10 especially. Furthermore, if the crystal layer 32 grows, as are shown in drawing 2 (c), and the border area of germanium island is sewn, the penetration transition

33 will be formed in the direction parallel to a substrate in the shape of a mesh.
[0032] Subsequently, non dope Si0.7 germanium0.3 which the amorphous layer crystallized completely and was eased If a buffer layer 12 is formed, as shown in drawing 2 (d), a disilane partial pressure will b returned to the usual epitaxial growth conditions (2.5xl0-2Pa), and the laminating of the carrier supply layer 13, the spacer layer 14, the channel layer 15, and the cap layers 16 and 17 will be carried out one by one.
[0033] Then, although the source, a drain, and the gate are formed in a wafer by ion implantation or metallization and FET is made, since these manufacture processes are generally used well, detailed explanation is omitted. However, it is necessary to suppress the upper limit temperature of a process at about 850 degrees C so that a distortion silicon layer may ease and transition may not occur.
[0034] In addition, in this operation gestalt, although the top used the usual CVD growth from the carrier supply layer, it is also possible for it to be amorphous, to form all the layers by the side of a front face from the start, and to crystallize from the transition conversion layer 11.
[0035] [2nd operation gestalt] drawing 5 is the cross section showing the important section composition of the semiconductor device concerning the 2nd operation gestalt of this invention. In addition, in drawing 5 , the same sign is given to the same portion as drawing 1 , and the detailed explanation is omitted. The semiconductor device of this operation gestalt is the CMOS inverter which used the distorted Si layer as p and an n channel.
[0036] n type germanium transition conversion layer 11a, n type relief Si0.7 germanium0.3-layer 12a, and n type distortion silicon layer 15a are formed on the n type Si substrate 10. And p type well is formed in a predetermined field of ion implantation, and it is p type germanium transition conversion layer 11b and p type relief Si0.7 germanium0.3. Layer 12b and p type distortion silicon layer 15b are formed. In addition, 55 is an insulator layer.
[0037] moreover, CMOS **** shown in drawing 5 -- bias of source 51a of pMOS and the n type relief layer 12a is carried out to 3V through wiring 57a, and source 52a of nMOS and p type relief layer 12b are connected to the ground through wiring 57c An input is applied to the gates 54a and 54b of both MOSs, and drain 51b of pMOS and drain 51b of nMOS become an output.
[0038] Since CMOS is the same composition as what is used for usual Si-CMOS except the structure of a substrate, it omits detailed explanation.
The [3rd operation gestalt] book operation gestalt shows the example using the MOS structure (HMOS) which has a channel at a hetero interface to a change of the usual MOS structure.
[0039] Drawing 6 is the cross section showing the important section composition of the semiconductor device which has the HMOS structure concerning the 3rd operation gestalt of this invention. In addition, in drawing 6 , the same sign is given to drawing 1 and the same portion as 5, and the detailed explanation is omitted.
[0040] What is necessary is just to insert p type distorted Si0.3 germanium0.7 layer (compressive strain) 61b of 5nm thickness between distorted Si layer 15b and the gate oxide film 53 about n-HMOS. p-HMOS -- being related -- n type Si0.3 germanium0.7 of 10nm of thickness of nHMOS and common use Layer 61a and distorted Si layer (hauling distortion) of 5nm of thickness 62a are inserted. [between / distorted Si layer 15a and the gate oxide films 53] In addition, it is distorted with distortion layer 61a, and the difference in thickness with layer 61b is a part to have been consumed by formation of the gate oxide film 53 of n-HMOS.
[0041] In this case, an n channel is distorted Si layer 15b and distorted Si0.3 germanium0.7. Near an interface with layer 61b, a p channel is distorted Si0.3 germanium0.7 again. It is formed between layer 61a and distorted Si layer 62a, respectively.
[0042] As a modification of this operation gestalt, it can also be fastidious using modulation dope structure as shown in the 1st operation gestalt. In this case, it is Si0.3 germanium0.7 to the upper part of p and an n channel. A spacer layer is minded and they are p type and n type Si0.3 germanium0.7. It is necessary to add a carrier supply layer.
[0043] In addition, this invention is not limited to the above-mentioned operation gestalt. For example, as a transition conversion layer, what is necessary is just Si1-x Gex (1>=x>0). Moreov r, as a buffer layer, what is necessary is just Si1-y Gey (x!=y). Moreover, as a channel layer, what is necessary is just Si1-z Gez (z!=y).
[0044] Besides the combination mentioned above, GaAs(1st semiconductor layer)/InAs(2nd

semiconductor layer)/InGaAs(3rd semiconductor layer)/InGaAs (distortion semiconductor layer), GaAs(1st semiconductor layer)/InP(2nd semiconductor layer)/InGaAsP(3rd semiconductor layer)/InGaAs (distortion semiconductor layer), Combination, such as InP(1st semiconductor layer)/InGaP(2nd semiconductor layer)/InGaP(3rd semiconductor layer)/InGaAs (distortion semiconductor layer), is possible. In addition, this invention is the range which does not deviate from the summary, and it deforms variously and it can be carried out.

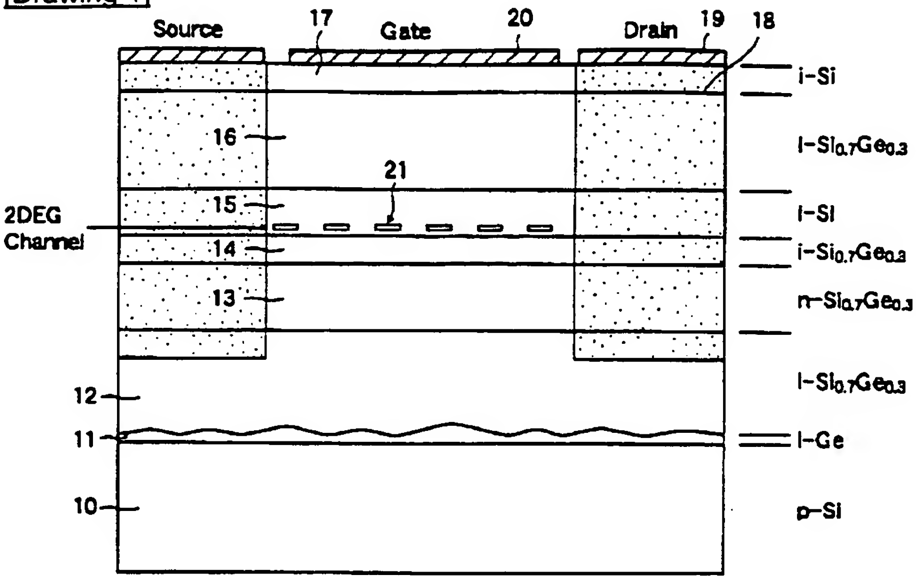
[Translation done.]

DESCRIPTION OF DRAWINGS

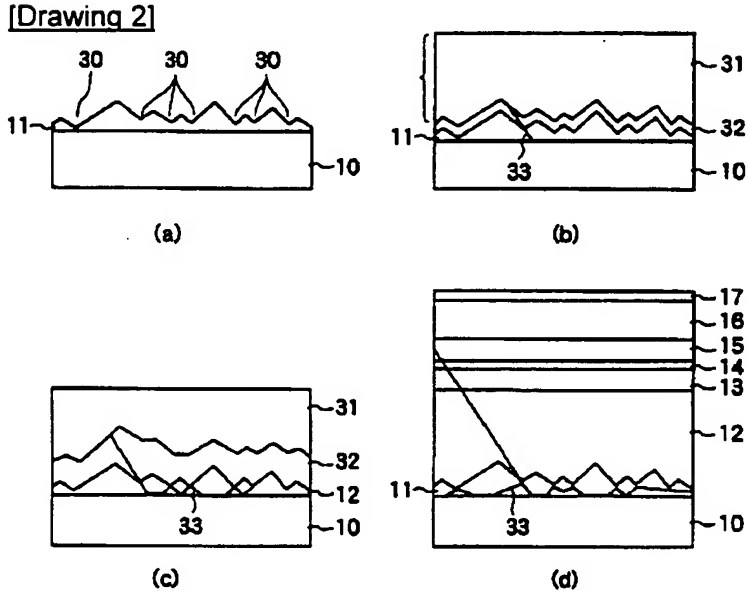
[Brief Description of the Drawings]
[Drawing 1] The cross section showing the composition of the semiconductor device concerning the 1st operation gestalt.
[Drawing 2] The process cross section showing the manufacturing process of the semiconductor device of drawing 1 .
[Drawing 3] Drawing showing the thickness distribution of germanium transition conversion layer.
[Drawing 4] Drawing for explaining the state of germanium transition conversion layer.
[Drawing 5] The cross section showing the composition of the semiconductor device concerning the 2nd operation gestalt.
[Drawing 6] The cross section showing the composition of the semiconductor device concerning the 3rd operation gestalt.
[Drawing 7] Drawing showing the electronic state near the Fermi surface of Si.
[Description of Notations]
10 -- Si substrate (1st semiconductor layer)
11 -- Transition conversion layer (the 2nd semiconductor layer, Si1-x Gex layer)
12 -- Si0.7 germanium0.3 Buffer layer (the 3rd semiconductor layer, Si1-y Gey layer)
13 -- Si0.7 germanium0.3 Carrier supply layer
14 -- Si0.7 germanium0.3 Spacer layer
15 -- Distorted Si channel layer (a distortion semiconductor layer, Si1-z Gez layer)
16 -- Si0.7 germanium0.3 Cap layer
17 -- Distorted Si cap layer
18 -- n type diffusion field
19 -- aluminum electrode
20 -- Schottky gate electrode

[Translation done.] DRAWINGS

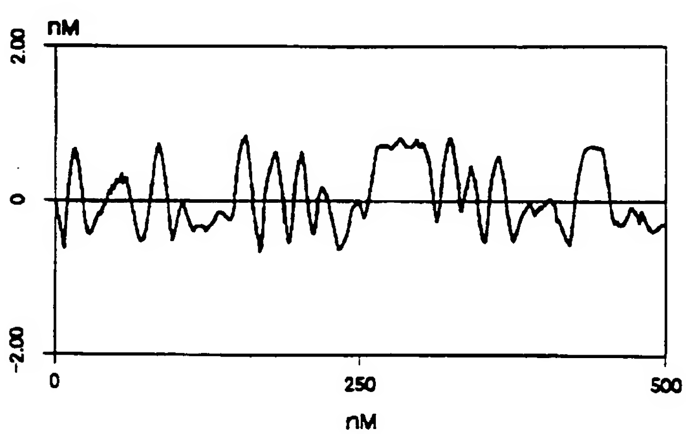
[Drawing 1]



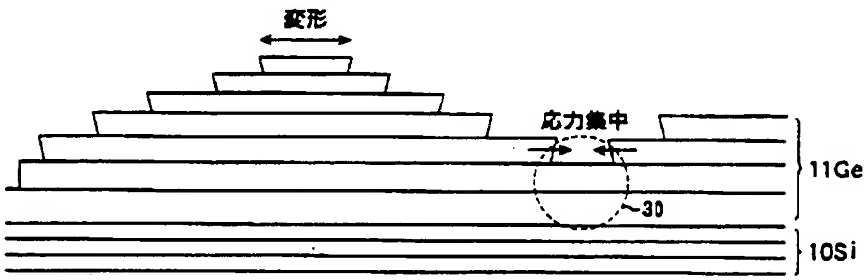
[Drawing 2]



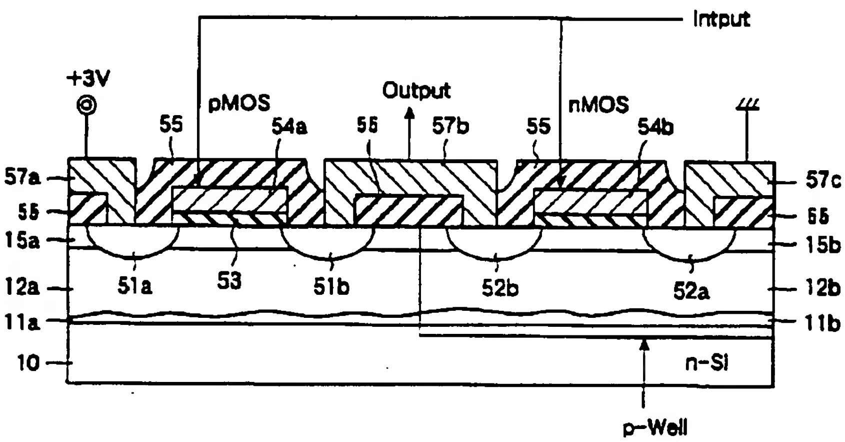
[Drawing 3]



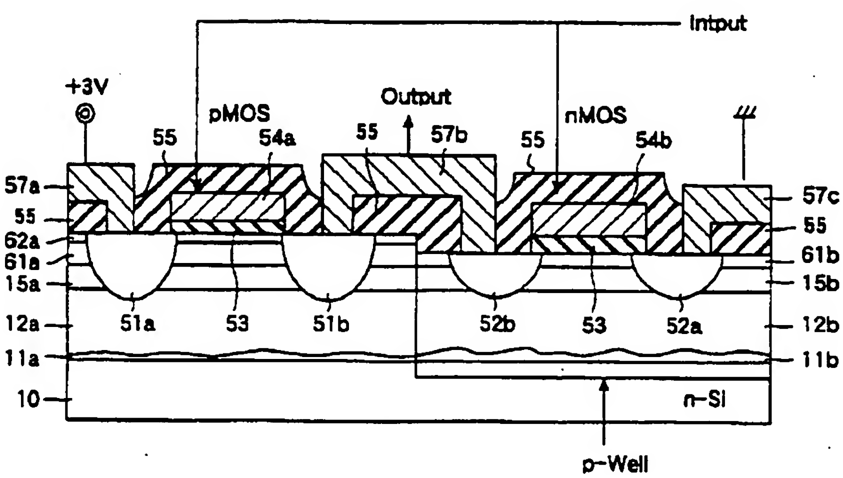
[Drawing 4]



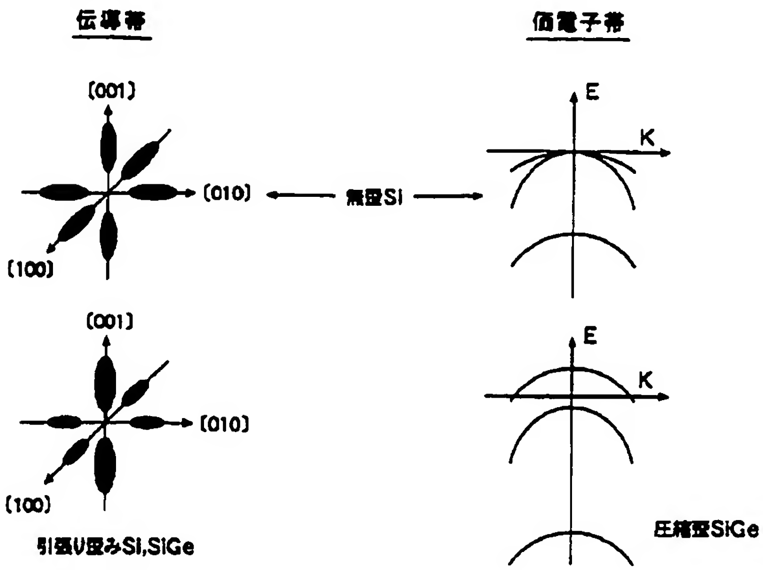
[Drawing 5]



[Drawing 6]



[Drawing 7]



[Translation done.]